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Metalorganic vapor phase epitaxial growth of (211)B CdTe on nanopatterned (211)Si

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Low-defect density epitaxial CdTe on Si is very crucial for fabricating high performance HgCdTe IR focal planar arrays on Si. This paper discusses a novel nanopatterning technique to explore defect reduction in CdTe epitaxy on (211)Si. Nanopatterning of full 3" (211)Si wafers was done by growing a thin layer of thermal SiO_2 and patterning by molecular transfer lithography (MxL) based on water-soluble templates. Conditions for obtaining selective Ge and CdTe were obtained in the temperature range of 575-675 °C and 505-520 °C respectively. X-ray analysis of thin CdTe films grown on these substrates gave wider full-width half-maximum (FWHM) values when compared to the layers grown on blanket (non-patterned) (211)Si, which is attributed to some patterning defects and spurious nucleation on oxide side walls.

1 Introduction Epitaxial growth of low defect density CdTe on Si is very critical in obtaining high crystal quality HgCdTe device layers for fabricating efficient IR focal planar arrays, which is the main motivation for the present work [1, 2]. However, low defect CdTe is also important in other applications such as solar cells and x-ray detectors [3, 4]. Growth of CdTe on Si has advantages such as availability of high quality large area wafers and low manufacturing costs. The use of Si also minimizes thermal mismatch issues with the signal readout Si chip. But the inherent challenge associated with HgCdTe/CdTe epitaxy on Si is the ~19% lattice mismatch which makes unavoidable, the generation of various defects, of which threading dislocations (TDs) propagating into the device layers have been observed to act as electron-hole pair recombination centres degrading the device performance [5]. With the progress achieved so far in CdTe epitaxy on Si, high quality CdTe can be obtained by molecular beam epitaxy (MBE) and metalorganic vapour phase epitaxy (MOVPE) with TD densities in the low-10^5 cm^{-2} range [6, 7]. TD density needs to be reduced by another order of magnitude for HgCdTe/Si based IR devices to operate efficiently in the long wavelength IR region.

Different approaches have been used to reduce TD density in CdTe/Si. One of the widely adopted techniques is the growth of thick CdTe buffer layers with *in-situ* thermal cyclic annealing which has been reported to give good results in terms of defect annihilation [8, 9]. Another approach consists of using patterned Si substrates where suitable growth windows are defined in SiO_2 masks [10-12]. Patterned windows help in reducing the defect levels in the epitaxial films primarily by reducing the length that some dislocations can glide to reach the edges of the growth windows where they get annihilated. Nanopatterning offers promise since the size of the windows is on the order of few nanometres depending on the patterning technique employed. Nanoheteroepitaxy (NHE) is a fundamentally novel approach where the patterned openings are < 20 nm

which gives rise to additional stress relief mechanisms [13]. But implementing NHE on a commercial scale is still challenging at the moment. In our present work, we have demonstrated a proof of principle of using nanopatterned (211)Si for MOVPE growth of selective epitaxial Ge and (211)B CdTe buffer layer structures.

2 Experimental procedures (211)B CdTe is the preferred orientation since it is the present industry standard in the US and it has been reported that epitaxial CdTe on (211)Si is immune to twin and hillock formation [14]. Nanopatterning of 3" SiO_2/(211)Si wafers was carried out at Transfer Devices Inc., using molecular transfer lithography (MxL) with water soluble templates to produce circular holes of ~380 nm and a pitch of ~540 nm. The details of this novel patterning technique have been described elsewhere [15, 16]. MxL technique is advantageous since it offers full wafer patterning and opportunities for further reduction in patterned dimensions uniformly on large area wafers. First, 60 nm thick thermal dry SiO_2 was grown on 3" diameter (211)Si wafers. Photoresist (PR) was applied and nanopatterned. The transfer of patterns from PR to the underlying SiO_2 was done at RPI by dry etching using CHF_3:O_2 mixture. Etching was intentionally stopped when the oxide thickness in the holes was in the range of 2-5 nm, which was removed by dipping in 1:30 HF:H_2O solution just before the reaction. Growth of Ge and CdTe was conducted in a low-pressure vertical cold-wall MOVPE reactor equipped with a rotating heater/substrate holder. Germane (1% in H_2) was the precursor for Ge and dimethyl cadmium (DMCd)/diisopropyl telluride (DiPTe) were the precursors for CdTe growth.

3 Results and discussion Figure 1 shows a scanning electron microscope (SEM) image of the nanopattern after SiO_2 dry etching and PR removal. A thin (2-5 nm) SiO_2 was intentionally left in the holes after dry etching to prevent any damage to the Si interface. A quick dip (40 s) of the wafers in dilute HF was done prior to starting the growth to remove any remaining oxide inside the holes. Before initiating Ge growth, As passivation of Si surface was carried out by flowing tertiarybutyl arsine (TBAs) during the reactor stabilization step which has been previously reported to help in preventing spurious nucleation of cross contaminants on Si and also help in getting higher quality Ge and CdTe epilayers on blanket (211)Si [17]. The most important part of this work was getting selective growth conditions for Ge and CdTe. A thin Ge layer was needed as it helped in lattice mismatch grading and also in improving the quality of subsequent CdTe layer. At the end of Ge growth, TBAs was introduced during cool down to CdTe growth temperatures to get the 'B' polarity of (211)CdTe.

Figures 2(a) and (b) show selective Ge on As passivated nanopatterned (211)Si at 575 °C and 675 °C respectively with pressure maintained at 150 Torr and total H_2 flow rate of 2.5 l/m. X-ray diffraction (XRD) confirmed fully relaxed Ge nanostructures. However it was observed that the top surface morphology of Ge inside the holes was rough compared to Ge growth of comparable thickness on blanket (211)Si. We attribute the surface roughness to some spurious nucleation occurring on the oxide sidewalls that may generate twinning and/or stacking faults. This may be the result of inefficient substrate cleaning prior to growth. Ways to overcome this problem is being worked upon presently. Figures 3(a) and (b) show growth of selective CdTe at 505 °C and 520 °C respectively over thin selective Ge (~20 nm). It was observed that higher temperatures and lower pressures were required for CdTe growth on nanopatterns compared to growing directly on blanket (211)Si. For example, when CdTe growth was made at 350 °C which is typically the temperature for growing high crystal quality CdTe on blanket Si, the growth on nanopatterned Si was non selective as shown in Fig. 4. In this regard, MOVPE technique is advantageous since it offers possibility for higher temperature CdTe growth.

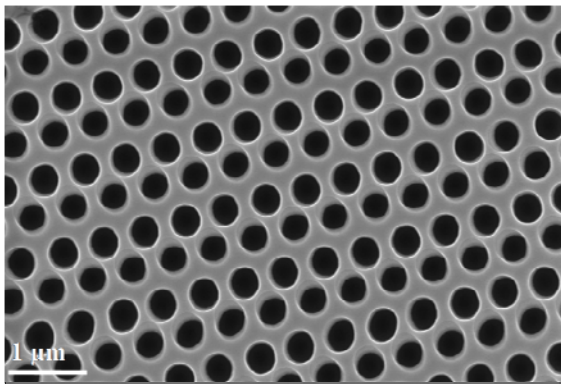

Figure 1 SEM image of nanopatterned (211)Si after SiO_2 dry etching and PR removal.

An effort was also made to grow thin uniformly merged ~0.6 µm (211)B CdTe film on nanopatterned (211)Si by using the selective Ge and CdTe conditions and allowing CdTe to completely merge. A schematic of the growth scheme is shown in Fig. 5. In this approach, Ge was grown inside the holes to the point when growths from adjacent holes were close to merging. (211)B CdTe was then grown on top of these Ge nanostructures, with 'B' polarity being achieved by passivating the Ge surface with As during cool down to CdTe growth temperature. XRD analysis confirmed fully relaxed single crystal nature of CdTe but the FWHM of (422)CdTe rocking curve was higher for the nanopatterned growth (2900 arc-s) compared to growth done on blanket (211)Si (472 arcs). One of the main reasons for degradation in crystal quality is the generation of additional defects when growth from adjacent patterned holes merge to form a thin layer. This is presently being investigated in more detail using transmission electron microscopy (TEM). Techniques like annealing the

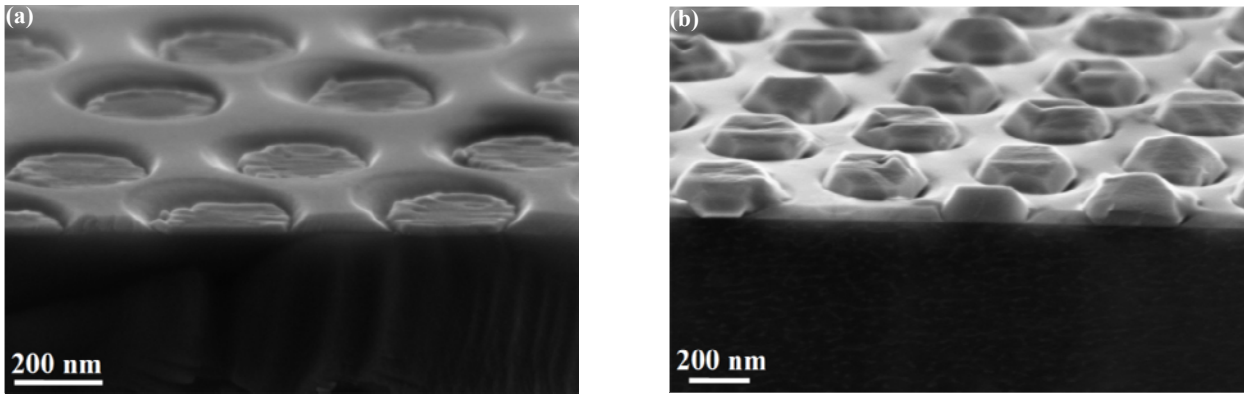

Figure 2 Selective Ge on nanopatterned (211)Si with As passivation of Si surface: (a) growth at 575 °C and (b) growth at 675 °C. Higher temperatures led to rougher surface morphology.

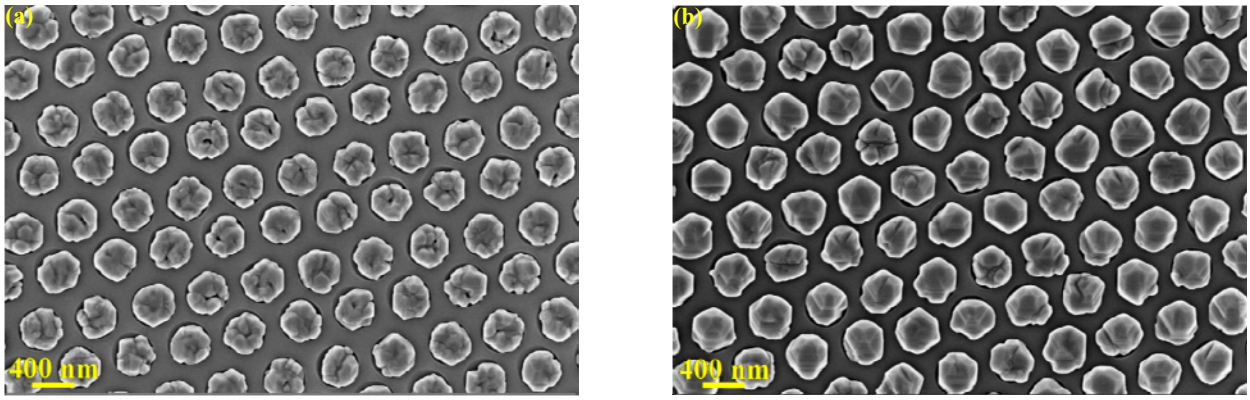

Figure 3 Selective CdTe on nanopatterned (211)Si with a thin intermediate selective Ge layer: (a) growth at 505 °C and (b) growth at 520 °C.

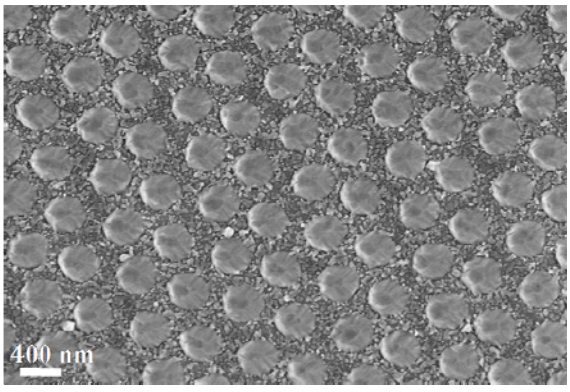

Figure 4 Non-selective CdTe on nanopatterned (211)Si at 350 °C growth temperature.

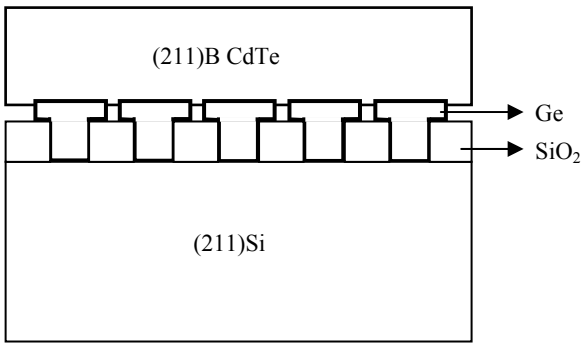

Figure 5 Schematic of growth scheme on nanopatterned (211)Si to get ~600 nm of (211)B CdTe.

films in the initial stages of growth could help in defect reduction and is presently being studied.

4 Conclusions A new approach to defect reduction in CdTe epitaxy on (211)Si has been explored using MxL. Conditions for obtaining selective Ge and CdTe epitaxy were first established. The presence of roughness indicates the occurrence of some spurious nucleation. An effort was made to grow thin CdTe films on the nanopatterned substrates. Initial results indicate additional defect generation when the islands from the patterns merged to form a thin layer.

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